HOLT INTEGRATED CIRCUITS INC.

August, 2022

HI-2579

3.3V MIL-STD-1553/1760 Dual Transceiver with Low Profile Integrated Transformers

GENERAL DESCRIPTION

The HI-2579 is a low power CMOS dual transceiver with integrated transformers designed to meet the requirements of the MIL-STD-1553 / MIL-STD-1760 specifications. The dual transceivers with integrated transformers provide a low profile single part solution for interfacing a protocol IC or FPGA to a dual redundant MIL-STD-1553 bus.

The transmitter section of each bus takes complementary CMOS / TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the integrated isolation transformer. Separate transmitter inhibit control signals are provided for each transmitter.

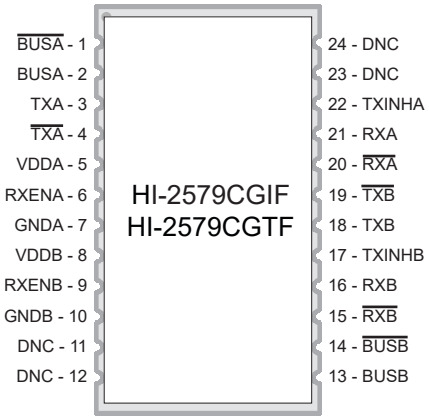
The receiver section of the each bus converts the 1553 bus differential data to complementary CMOS / TTL data suitable for inputting to a Manchester decoder. Each receiver has a separate enable input which can be used to force both receiver outputs to logic “0”.

The family of parts are available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges.

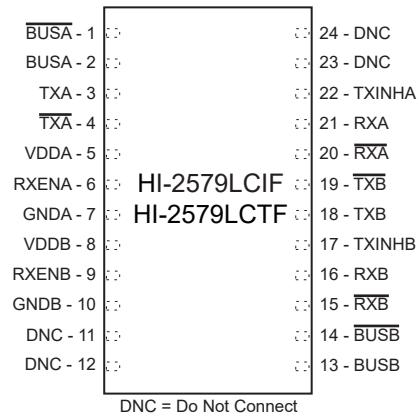
FEATURES

- Dual-redundant MIL-STD-1553 transceivers with integrated transformers
- Small footprint and low profile package
- Compliant to MIL-STD-1553A and B, MIL-STD-1760, ARINC 708A
- 3.3V single supply operation
- Less than 1.0W maximum power dissipation
- Industrial and extended temperature ranges

PIN CONFIGURATIONS (TOP)



DNC = Do Not Connect



DNC = Do Not Connect

BLOCK DIAGRAM

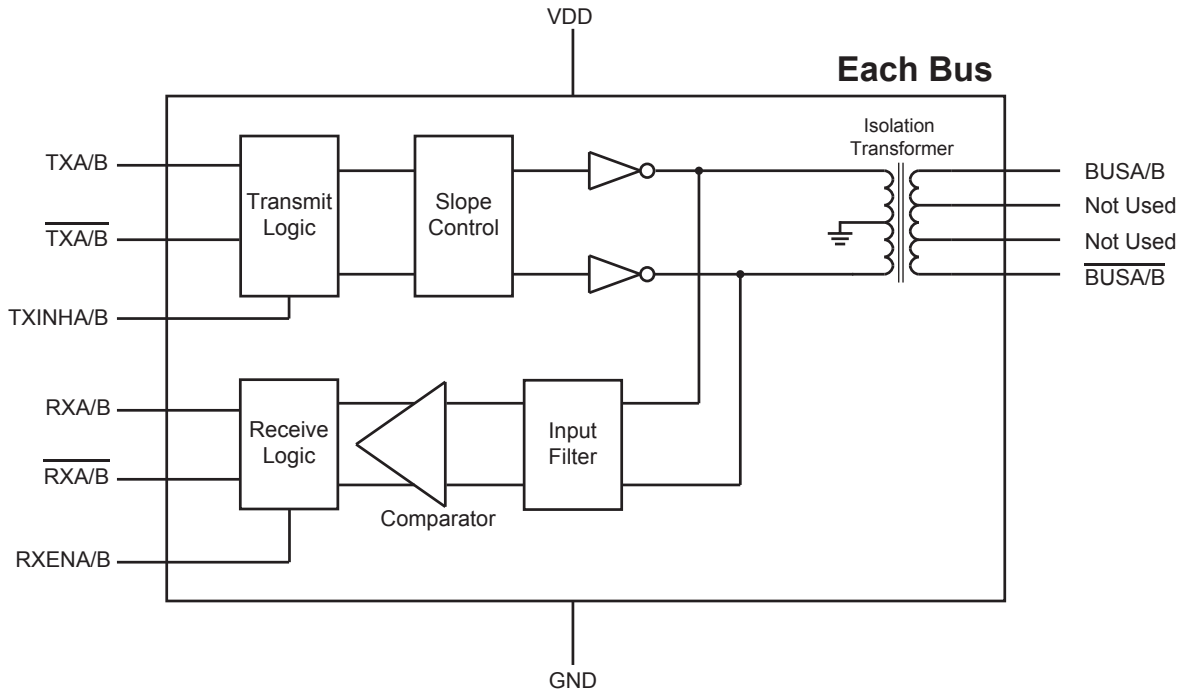


Figure 1. Block Diagram

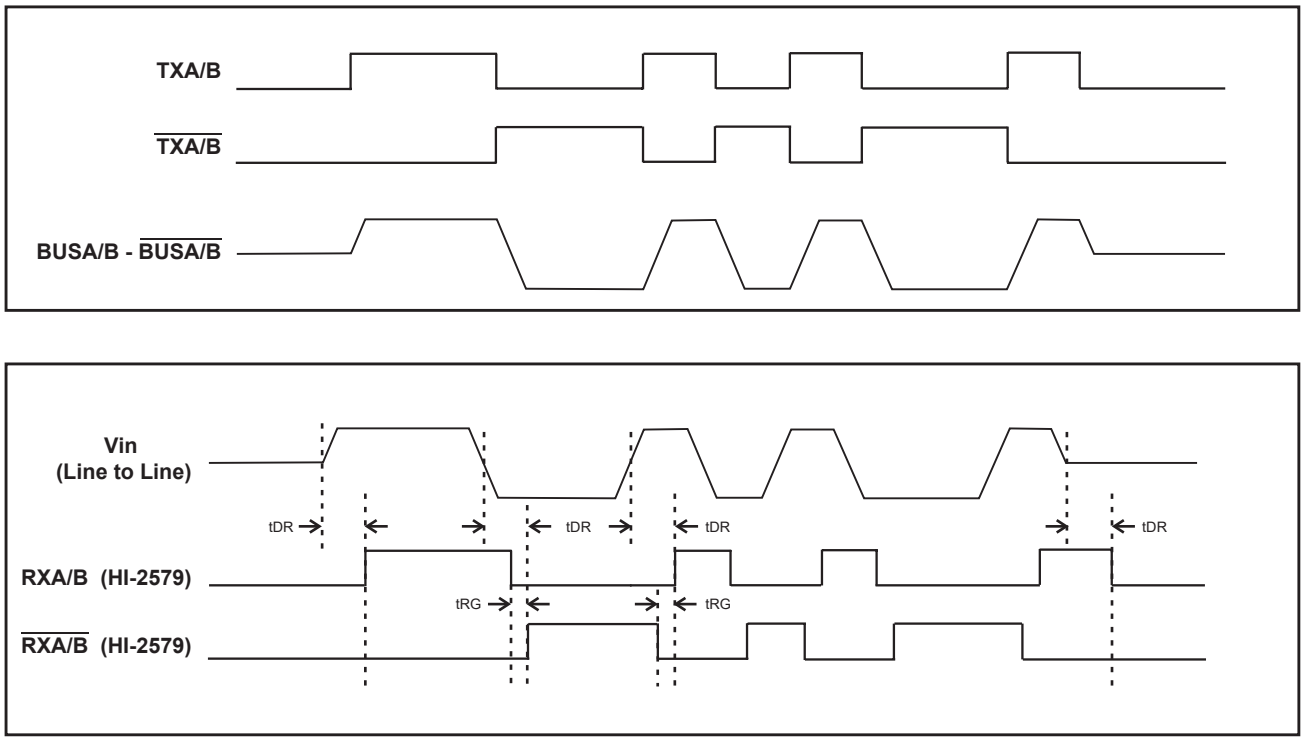


Figure 2. Example Waveforms

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Pin	Symbol	Function	Description
1	$\overline{\text{BUSA}}$	Analog O/P	MIL-STD-1553 Bus A driver, negative signal (Transformer coupled or direct coupled bus connections)
2	BUSA	Analog O/P	MIL-STD-1553 Bus A driver, positive signal (Transformer coupled or direct coupled bus connections)
3	TXA	Digital I/P	Transmitter A digital data input, non-inverted
4	$\overline{\text{TXA}}$	Digital I/P	Transmitter A digital data input, inverted
5	VDDA	Power	Transceiver A 3.3V supply
6	RXENA	Digital I/P	Receiver A enable. If low, forces both RXA and $\overline{\text{RXA}}$ low
7	GNDA	Power	Transceiver A ground connection
8	VDDB	Power	Transceiver B 3.3V supply
9	RXENB	Digital I/P	Receiver B enable. If low, forces both RXB and $\overline{\text{RXB}}$ low
10	GNDB	Power	Transceiver B ground connection
11	DNC	–	Not Used. Do Not Connect.
12	DNC	–	Not Used. Do Not Connect.
13	BUSB	Analog O/P	MIL-STD-1553 Bus B driver, positive signal (Transformer coupled or direct coupled bus connections)
14	$\overline{\text{BUSB}}$	Analog O/P	MIL-STD-1553 Bus B driver, negative signal (Transformer coupled or direct coupled bus connections)
15	$\overline{\text{RXB}}$	Digital O/P	Receiver B output, inverted
16	RXB	Digital O/P	Receiver B output, non-inverted
17	TXINHB	Digital I/P	Transmit inhibit, Bus B. If high BUSB, $\overline{\text{BUSB}}$ outputs are disabled
18	TXB	Digital I/P	Transmitter B digital data input, non-inverted
19	$\overline{\text{TXB}}$	Digital I/P	Transmitter B digital data input, inverted
20	$\overline{\text{RXA}}$	Digital O/P	Receiver A output, inverted
21	RXA	Digital O/P	Receiver A output, non-inverted
22	TXINHA	Digital I/P	Transmit inhibit, Bus A. If high BUSA, $\overline{\text{BUSA}}$ outputs are disabled
23	DNC	–	Not Used. Do Not Connect.
24	DNC	–	Not Used. Do Not Connect.

FUNCTIONAL DESCRIPTION

The HI-2579 family of data bus transceivers contains differential voltage source drivers, differential receivers and integrated transformers. They are intended for applications using a MIL-STD-1553 A/B data bus.

Transmitter

Data is input to the device's transmitter section from the complementary CMOS inputs TXA/B and $\overline{\text{TXA/B}}$. The transmitter accepts Manchester II bi-phase data and converts it to differential voltages which drive the internal transformers on BUSA/B and $\overline{\text{BUSA/B}}$. The transformer outputs are either direct or transformer coupled to the MIL-STD-1553 data bus. Both coupling methods produce a nominal voltage on the main bus of 7.5 volts peak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when both TXA/B and $\overline{\text{TXA/B}}$ are either at a logic "1" or logic "0" simultaneously. A logic "1" applied to the TXINHA/B input forces the transmitter to the high impedance state, regardless of the state of TXA/B and $\overline{\text{TXA/B}}$.

Receiver

The receiver accepts bi-phase differential data from the MIL-STD-1553 bus through the same direct or transformer coupled interface as the transmitter. The receiver's differential input stage includes a filter and threshold comparator that produces CMOS data at the RXA/B and $\overline{\text{RXA/B}}$ output pins. When the MIL-STD-1553 bus is idle and RXENA or RXENB are high, RXA/B will be logic "0".

Each set of receiver outputs can also be independently forced to the bus idle state (logic "0") by setting RXENA or RXENB low.

MIL-STD-1553 Bus Interface

There are two ways of connecting to the MIL-STD-1553 bus, using a direct coupled interface or a transformer coupled interface (see Figure 3).

A direct coupled interface uses the internal 1:2.5 ratio isolation transformer and two 55Ω isolation resistors between the transformer and the bus.

In a transformer coupled interface, the transceiver is connected to the internal 1:2.5 isolation transformer which in turn is connected to a 1:1.4 coupling transformer. The transformer coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedance (Zo) between the coupling transformer and the bus. The coupling transformer and coupling resistors are commonly integrated in a single device known as a stub coupler.

Figure 4 and Figure 5 show test circuits for measuring electrical characteristics of both direct and transformer coupled interfaces respectively (see "Electrical Characteristics" on the following pages) .

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	-0.3 V to +5 V
Logic input voltage range	-0.3 V DC to +3.6 V
Receiver differential voltage	50 Vp-p
Driver peak output current	+1.0 A
Power dissipation at 25°C	1.0 W
Solder Temperature	245°C max.
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	V_{DD} 3.3V ± 5%
Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: *Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.*

ELECTRICAL CHARACTERISTICS

Table 2. DC Electrical Characteristics

V_{DD} = +3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage		V_{DD}		3.15	3.3	3.45	V
Total Supply Current		I_{CC1}	Not Transmitting		4	17	mA
		I_{CC2}	Transmit one bus @ 50% duty cycle		225	320	mA
		I_{CC3}	Transmit one bus @ 100% duty cycle		425	640	mA
Power Dissipation		P_{D1}	Not Transmitting			0.06	W
		P_{D2}	Transmit one bus @ 100% duty cycle		0.5	1.0	W
Min. Input Voltage (HI)		V_{IH}	Digital Inputs	2.0			V
Max. Input Voltage (LO)		V_{IL}	Digital Inputs			30%	V_{DD}
Min. Input Current (HI)		I_{IH}	Digital Inputs			20	µA
Max. Input Current (LO)		I_{IL}	Digital Inputs	-20			µA
Min. Output Voltage (HI)		V_{OH}	I_{OUT} = -1.0mA, Digital Outputs	90%			V_{DD}
Max. Output Voltage (LO)		V_{OL}	I_{OUT} = +1.0mA, Digital Outputs			10%	V_{DD}
RECEIVER (Measured at Point "AD" in Figure 4 unless otherwise specified)							
Input Resistance		R_{IN}	Differential	2			kΩ
Input Capacitance		C_{IN}	Differential			5	pF
Common Mode Rejection Ratio		CMRR		45			dB
Input Common Mode Voltage		V_{ICM}		-10.0		+10.0	V-pk
Threshold Voltage - Direct Coupled	Detect	V_{THD}	1MHz Sine Wave (measured at point "AD" in Figure 4) RXA/B, $\overline{\text{RXA/B}}$ pulse width > 70 ns	1.15			Vp-p
	No Detect	V_{THND}	No pulse at RXA/B, $\overline{\text{RXA/B}}$			0.28	Vp-p
Threshold Voltage - Transformer Coupled	Detect	V_{THD}	1MHz Sine Wave (measured at point "AT" in Figure 5) RXA/B, $\overline{\text{RXA/B}}$ pulse width > 70 ns	0.86			Vp-p
	No Detect	V_{THND}	No pulse at RXA/B, $\overline{\text{RXA/B}}$			0.20	Vp-p

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
TRANSMITTER (Measured at Point "AD" in Figure 4 unless otherwise specified)							
Output Voltage	Direct Coupled	V_{OUT}	35Ω Load (measured at point "AD" in Figure 4)	6.1		9.0	Vp-p
	Transformer Coupled	V_{OUT}	70Ω Load (measured at point "AT" in Figure 5)	20.0		27.0	Vp-p
Output Noise		V_{ON}	Differential, Inhibited			10	mVp-p
Output Dynamic Offset Voltage	Direct Coupled	V_{DYN}	35Ω Load (measured at point "AD" in Figure 4)	-90		+90	mV
	Transformer Coupled	V_{DYN}	70Ω Load (measured at point "AT" in Figure 5)	-250		+250	mV
Output Capacitance		C_{OUT}	1MHz Sine Wave			15	pF

Table 3. AC Electrical Characteristics

V_{DD} = +3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RECEIVER (Measured at Point "AT" in Figure 5)						
Receiver Delay	t_{DR}	From input zero crossing to RXA/B or $\overline{RXA/B}$			450 Note 3	ns
Receiver Gap Time	t_{RG}	Spacing between RXA/B and $\overline{RXA/B}$ pulses	90 Note 1		365 Note 2	ns
Receiver Enable Delay	t_{REN}	From RXENA/B rising or falling edge to RXA/B or $\overline{RXA/B}$			40	ns
TRANSMITTER (Measured at Point "AD" in Figure 4)						
Driver Delay	t_{DT}	TXA/B, TXA/B to BUSA/B, BUSA/B			150	ns
Rise Time	t_r	35Ω Load	100		300	ns
Fall Time	t_f	35Ω Load	100		300	ns
Inhibit Delay	t_{DI-H}	Inhibited Output			100	ns
	t_{DI-L}	Active Output			150	ns

Note 1. Measured using a 1 MHz sinusoid, 20 V peak to peak, line to line at point "AT" (Guaranteed but not tested).

Note 2. Measured using a 1 MHz sinusoid, 860 mV peak to peak, line to line at point "AT" (100% tested).

Note 3. Measured using a 1 MHz sinusoid, 860 mV peak to peak, line to line at point "AT". Measured from input zero crossing point.

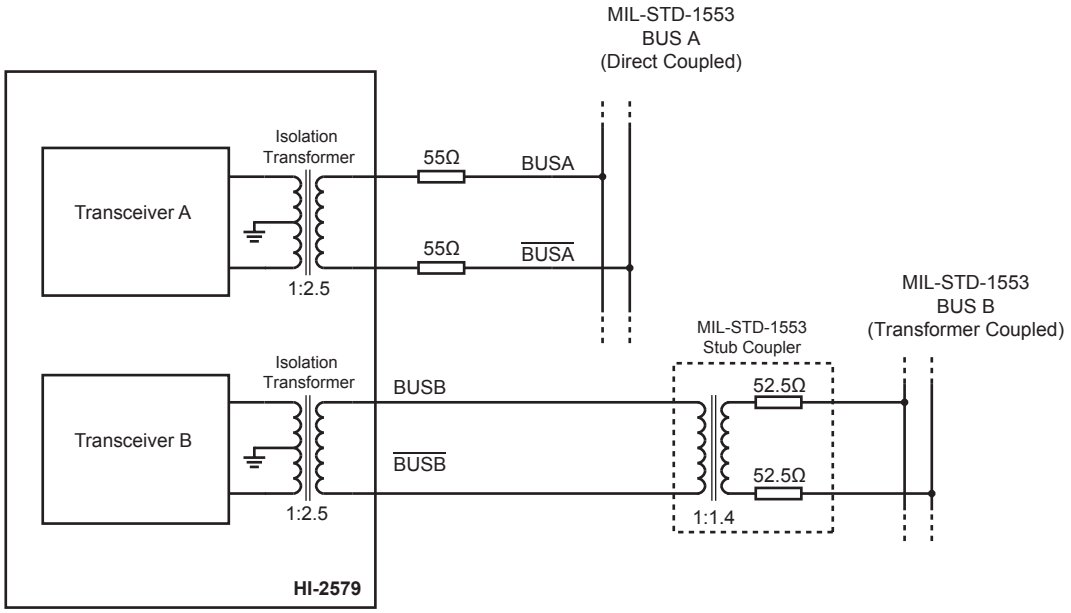


Figure 3. Bus Connections Example using HI-2579

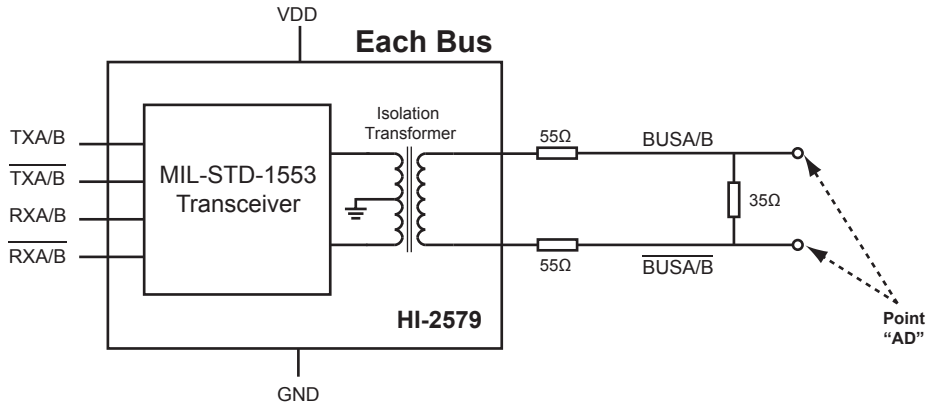


Figure 4. Direct Coupled Test Circuit

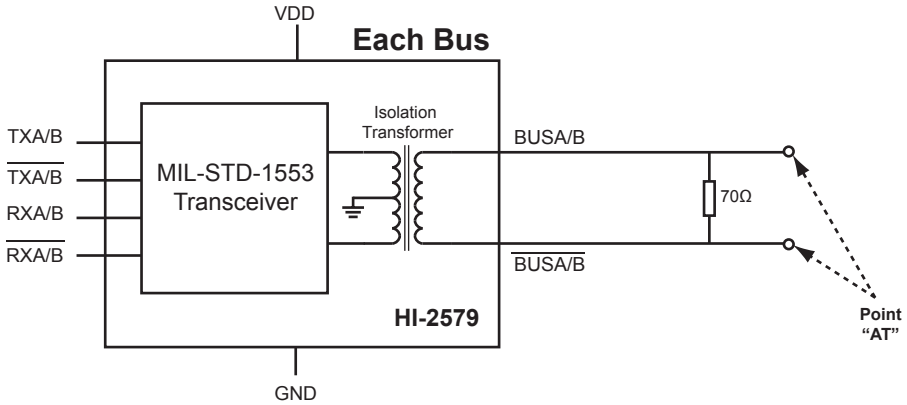


Figure 5. Transformer Coupled Test Circuit

ORDERING INFORMATION

HI - 2579 CG x F **Ceramic Substrate**

PART NUMBER	LEAD FINISH
F	Pb-free, RoHS compliant

PART NUMBER	TEMPERATURE RANGE	FLOW	LEAD FINISH
I	-40°C to +85°C	I	Gold
T	-55°C to +125°C	T	Gold

HI - 2579 LC x F **High TCE Substrate**

PART NUMBER	LEAD FINISH
F	Pb-free, RoHS compliant

PART NUMBER	TEMPERATURE RANGE	FLOW	LEAD FINISH
I	-40°C to +85°C	I	Gold
T	-55°C to +125°C	T	Gold

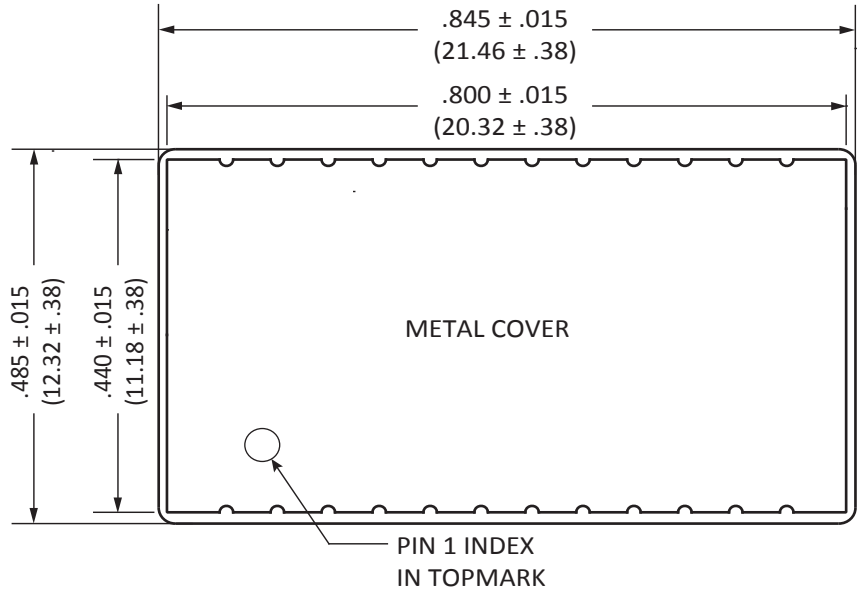
REVISION HISTORY

Revision		Date	Description of Change
DS2579,	Rev. New	10/8/2012	Initial Release
	Rev. A	5/23/2013	Correct Note 1 on package dimensions to state that the Heatsink pad is connected internally to ground.
	Rev. B	1/13/2015	Add “CG” low profile package option. Make minor clarifications and correct typographical errors in “DC Electrical Characteristics” and “AC Electrical Characteristics”. Corrected Receiver Threshold Voltage for Direct Coupled connection from 0.86V to 1.15V in “DC Electrical Characteristics”.
	Rev. C	3/5/2015	Clarify dimensions on package bottom-side test pads. No change in physical dimensions. Remove “CL” package option.
	Rev. D	3/27/2015	Correct typos in Pin Descriptions table. Correct bus connections in Figure 3 and Figure 4.
	Rev. E	07/29/2016	“Table 2. DC Electrical Characteristics”: change V_{IH} to 2.0V min.
	Rev. F	07/28/2017	Clarify labeling of “keep out” zones and heatsink on package drawing. Update package photo.
	Rev. G	02/22/2019	Add “LC” high TCE substrate package variant.
	Rev. H	08/18/2022	Remove HI-2581 part variant.

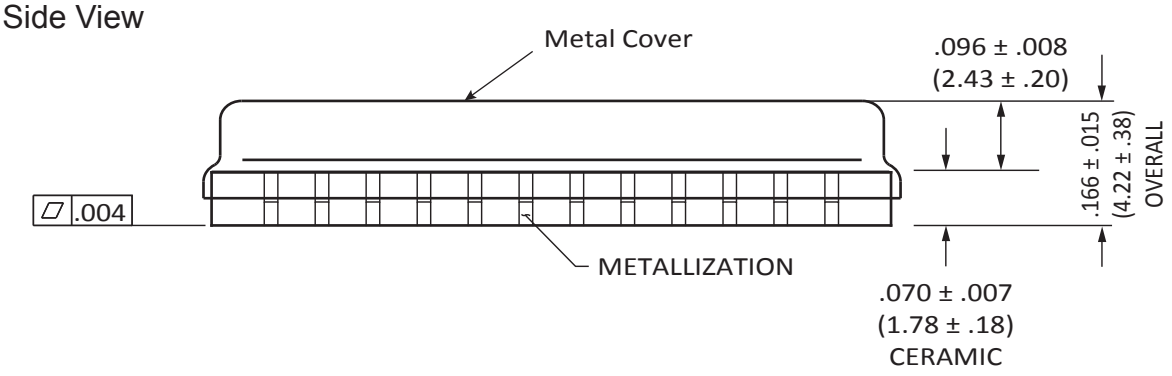
PACKAGE DIMENSIONS - “CG” CERAMIC SUBSTRATE

Top View

Dimensions in inches (mm)



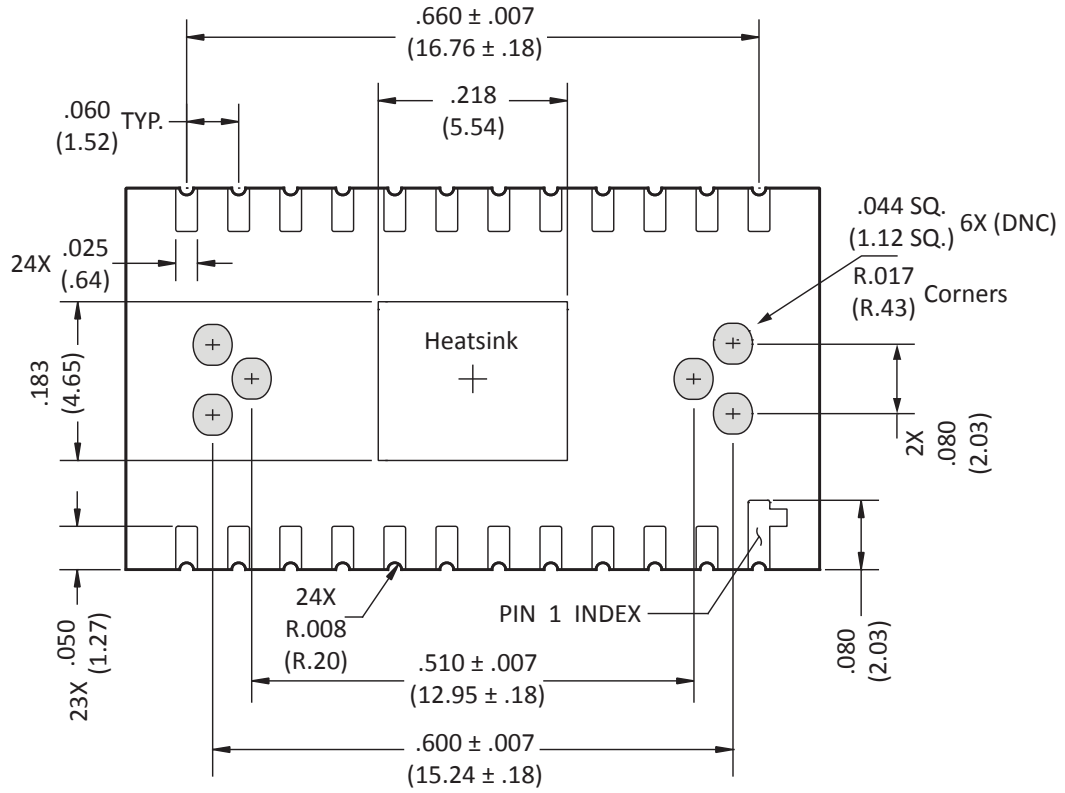
Side View



PACKAGE DIMENSIONS - “CG” CERAMIC SUBSTRATE

Bottom View

Dimensions in inches (mm)



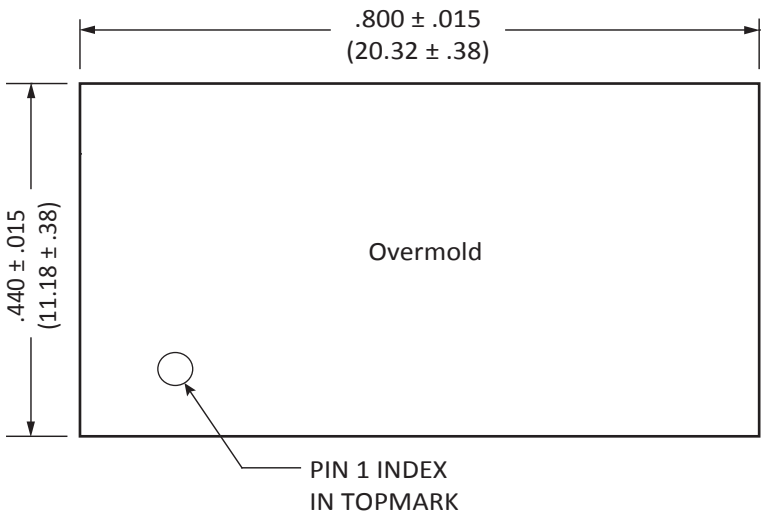
Notes:

1. Heatsink pad is internally connected to device GND pins. Connection to external GND for heat extraction is not necessary.
2. The “keep out” zones (shaded grey) enclose test pads for the transformer primary windings. DO NOT CONNECT (DNC).
3. Routing traces under the six test pads is not recommended.

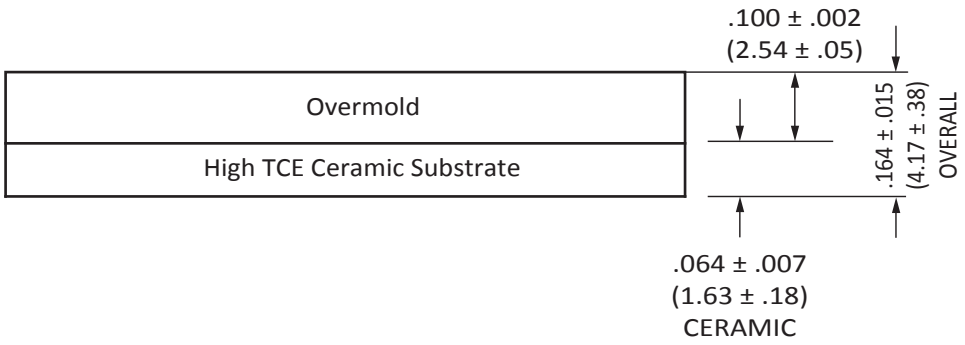
PACKAGE DIMENSIONS - “LC” HIGH TCE SUBSTRATE

Top View

Dimensions in inches (mm)



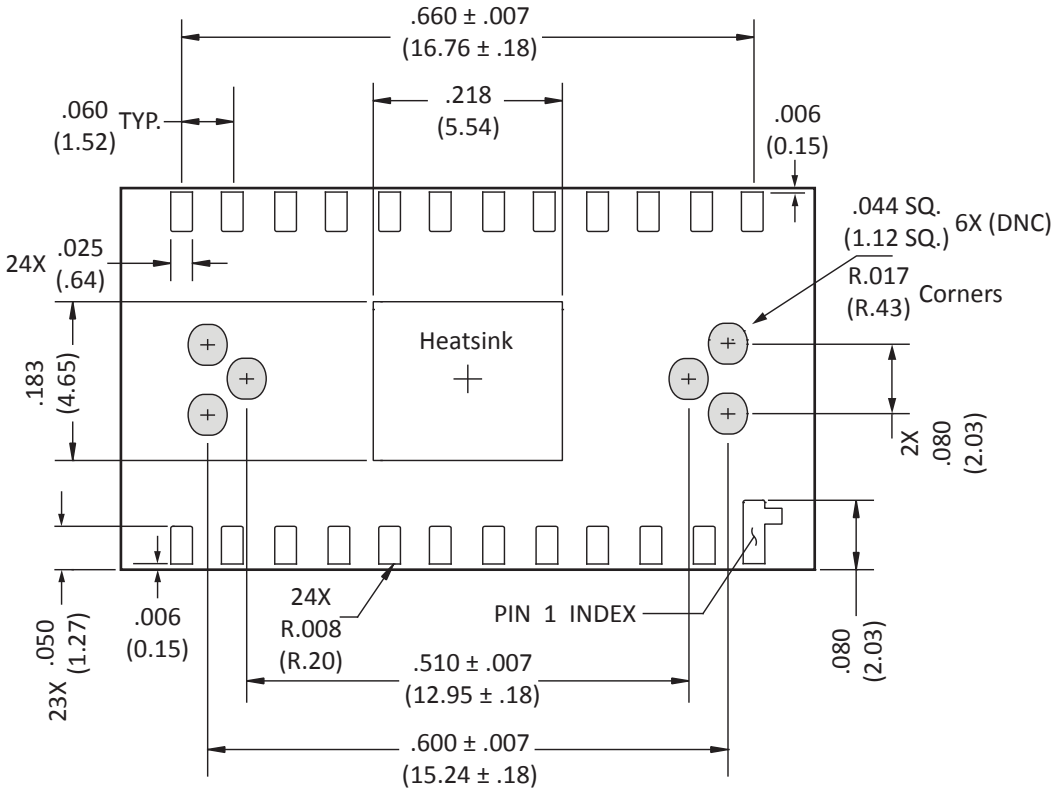
Side View



PACKAGE DIMENSIONS - “LC” HIGH TCE SUBSTRATE

Bottom View

Dimensions in inches (mm)



Notes:

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